ISO7816 UART

Product Specification

Disclaimer

Systemyde International Corporation reserves the right to make changes at any time, without notice, to improve design or performance and provide the best product possible. Systemyde International Corporation makes no warrant for the use of its products and assumes no responsibility for any errors which may appear in this document nor does it make any commitment to update the information contained herein.

Systemyde International Corporation products are not authorized for use in life support devices or systems. Nothing contained herein shall be construed as a recommendation to use any product in violation of existing patents, copyrights or other rights of third parties. No license is granted by implication or otherwise under any patent, patent rights or other rights, of Systemyde International Corporation. All trademarks are trademarks of their respective companies.

Every effort has been made to ensure the accuracy of the information contain herein. If you find errors or inconsistencies please bring them to our attention. In all cases, however, the Verilog HDL source code for the iso7816 design defines “proper operation”.

Table of Contents

This page intentionally left blank.

Overview

The ISO7816 UART contains all of the digital logic necessary to communicate with an ISO/IEC 7816 or EMV 4.3 integrated circuit card. The design separates the control registers and bus interface from the core logic, which allows you to redefine the register interface to meet your specific requirements.

General Features:

- Technology-independent Verilog HDL implementation.
- 8-bit APB host interface.
- 8-byte receive buffer.
- 8-bit divider for generating card CLK signal from APB clock.
- Flexible multi-mode timers to handle the various ISO7816 time limits.
- Sampling of card serial data consistent with ISO7816 specification.

ISO7816/EMV4.3 Features:

- Protocol state machine to reduce CPU overhead. Time limits set by compile option.
- Automatic initial character TS recognition.
- T=0 and T=1 protocols. T=0 protocol includes automatic retry (programmable limit).
- Dedicated CWT timer.
- Dedicated BWT timer.

This page intentionally left blank.

Signal Descriptions

The ISO7816 UART sits between a host and an integrated circuit card, and translates between the parallel 8-bit bus of the host and the bidirectional serial signals of the card. None of the ISO7816 UART signals are bidirectional, but will require external (to the UART) 3-state buffers to create true bidirectional signals.

The native host interface is eight bits wide, but it is easy to convert this interface to use sixteen or even thirty-two bits.

The ISO7816 UART is configured and controlled via a set of registers, but in many cases these registers can be replaced by hard-wired values if necessary to reduce gate count.

Card Interface group:

C_CLK (output, active-High). The Card Clock signal is derived from the Peripheral Clock. Initially the Card Clock should be 1MHz, but can be increased under software control if supported by the card.

C_C4IN (input). The Card C4 signal is undefined in ISO7816, but may be used by non-standard cards as an input, output or bidirectional signal. This is the input from pin C4.

C_C4OUT (output). The Card C4 signal is undefined in ISO7816, but may be used by non-standard cards as an input, output or bidirectional signal. This is the output for pin C4.

C_C6IN (input). The Card C6 signal is undefined in ISO7816, but may be used by non-standard cards as an input, output or bidirectional signal. This is the input from pin C6.

C_C6OUT (output). The Card C6 signal is undefined in ISO7816, but may be used by non-standard cards as an input, output or bidirectional signal. This is the output for pin C6.

C_C8IN (input). The Card C8 signal is undefined in ISO7816, but may be used by non-standard cards as an input, output or bidirectional signal. This is the input from pin C8.

C_C8OUT (output). The Card C8 signal is undefined in ISO7816, but may be used by non-standard cards as an input, output or bidirectional signal. This is the output for pin C8.

C_DIN (input). The Card Data Input signal is the card I/O signal (C7).

C_DOUT (output). The Card Data Output signal is the serial data output for the card. When the Card Data Output signal is Low, the card I/O signal (C7) should be driven Low. At all other times the card I/O signal should be pulled High passively. The Card Data Output signal is Low until the card activation sequence is started and will return Low when the card is deactivated.

C_PRES (input, active High). The Card Present signal should come from a mechanical card-present switch. This signal should be High when a card is present and Low when no card is present. If the Card Present signal goes Low the deactivation sequence will be automatically initiated.

C_RST (output, active High). The Card Reset signal is the master reset for the card. When the Card Reset signal is Low, the card RST signal (C2) should be driven Low. The Card Reset signal is Low until the card activation sequence is started and will return Low when the card is deactivated.

C_VCC18 (output, active High). The Card 1.8V Power Select signal should be used to select 1.8V for the card power supply.

C_VCC30 (output, active High). The Card 3.0V Power Select signal should be used to select 3.0V for the card power supply.

C_VCC50 (output, active High). The Card 5.0V Power Select signal should be used to select 5.0V for the card power supply. The card Power Select outputs are guaranteed to be mutually exclusive. The default selection is 5.0V.

C_VCCOK (input, active High). The Card Power Okay signal should be active when the card power supply is stable within spec. If the Card Power Okay signal goes Low the deactivation sequence will be automatically initiated.

C_VCCON (output, active High). The Card Power On signal should enable an external power supply to power to the card. The Card Power On signal is Low until the card activation sequence is started and will return Low when the card is deactivated.

Host Interface group:

PADDR[4:0] (inputs). The Address Bus selects the register, according to the table below:

PADDR	Register
00000	Master Control
00001	Direct Control/Status
00010	Clock Divider
00011	Clock Control
00100	EUT Width
00101	ETU Divider
00110	FIFO Control
00111	Parity Error Limit
01000	Time Constant 0, Byte 0
01001	Time Constant 0, Byte 1
01010	Time Constant 0, Byte 2
01011	Guard Time
01100	Time Constant 1, Byte 0
01101	Time Constant 1, Byte 1
01110	Time Constant 1, Byte 2
01111	Timer Control
10000	Master Mode
10001	Power Control
10010	Protocol State
10011	UART Status
10100	Protocol Interrupt Enable
10101	UART Interrupt Enable
10111	Parity Error Status
11010	Alternate Protocol State
11011	Alternate UART Status
11100	UART Buffer
11110	Version
11111	Master Reset

PCLK (input, active-High). The Peripheral Clock signal drives both the bus interface and serial interface portions of the design.

PENABLE (input, active-High). The Peripheral Enable signal strobes the data into or out of the device.

PINT_REQ (output, active High). The Interrupt Request signal is active when the device is requesting an interrupt. The specific type of interrupt request can be found

by reading the Protocol State and UART Status register. This output will be de-asserted when the interrupting condition has been removed.

PRDATA[7:0] (outputs). The Peripheral Read Data Bus is used to transfer data from the device to the host. This data bus is normally driven with all zeros, and will only be valid while both the Peripheral Enable and Peripheral Select signals are active and the Peripheral Write signal is inactive.

PRESETB (input, active-Low). The Master Reset signal completely initializes the device.

PSEL (input, active-High). The Peripheral Select signal enables the device for data transfer to or from the host.

PWDATA[7:0] (inputs). The Peripheral Write Data Bus carries write data from the host to the device. This bus is sampled by the device when the Peripheral Enable, Peripheral Select, and Peripheral Write signals are all active.

PWRITE (input, active-High). The Peripheral Write signal selects the direction for data transfer between the host and the device. High enables a write from the host to the device, while Low enables a read from the device by the host.

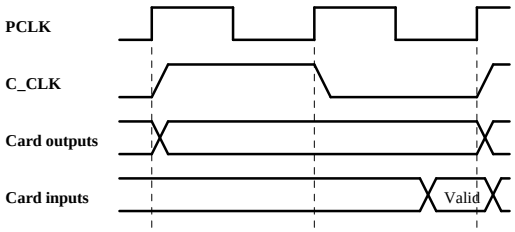
Miscellaneous group:

ETU_PLS (output, active High). The Elementary Time Unit Pulse signal is a one PCLK wide pulse that signals the serial bit rate. This signal is used by the transmitter to output transmit bits, but can also be used if additional ETU timers are necessary external to the UART. This signal is output continuously as long as C_RST is High, even if the Card Clock is stopped.

TEST_EN (input, active High). The Test Enable signal overrides the built-in time constants for the C_RST Low time to reduce the time required for simulation and test. Enabling test mode masks the upper eight bits of both the RST_EXIT_DLY and WARM_EXIT_DLY time constants, so that only the lower eight bits of these time constants are used. Enabling test mode also modifies Timer 0 and Timer 1 so that the increment starts at bit 8, rather than at bit 0.

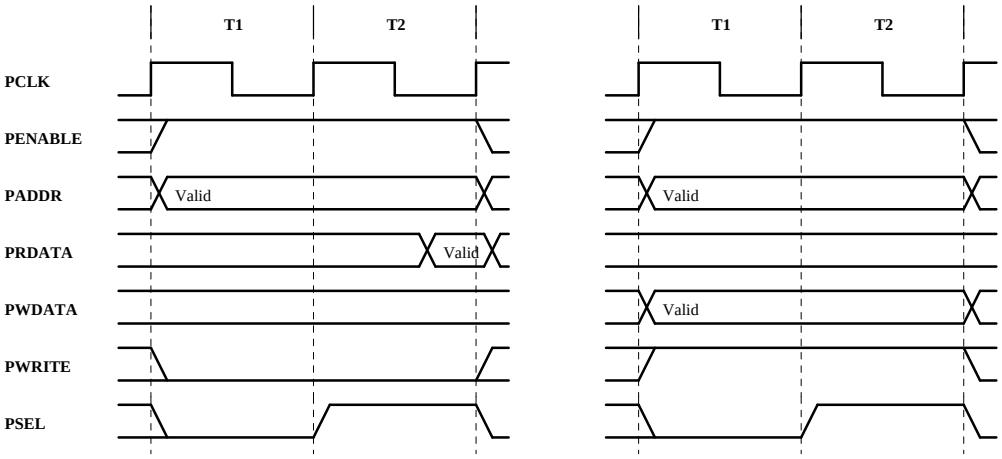
External Timing

The ISO7816 UART uses the PCLK signal for all timing. As shown in the figure below, all card outputs change relative to the rising edge of the PCLK signal and all card inputs are sampled by the rising edge of the PCLK signal. This figure shows the default case when the C_CLK signal is the PCLK signal divided by two. If the C_CLK signal is not active, the card outputs can change on any PCLK rising edge.



Host Interface Timing

Read and write transactions are shown in the figure below. Back-to-back transactions, of either type, are allowed.



Card Interface Timing:

The standards ISO/IEC 7816-3:2006 and EVM 4.3 (which uses ISO/IEC as a starting point) both specify a number of time values. In most cases these time values are identical, but in some cases EVM sets a constraint where ISO/IEC imposes no limit. In those cases where there is a difference, the EVM limit either guarantees a finite response time limit for the card, or a generous minimum time for the card to recover.

In the ISO7816 UART, many of these time values are set by logic-synthesis-time values that are consistent with the EVM specification. If your application does not require EVM compliance, these values can be changed before logic synthesis time. These constants can also be replaced by programmable values if required.

These time values, and the associated protocol controller, significantly reduce the CPU overhead required for certain card operations. Card activation and cold reset, warm reset, card deactivation, and clock stop all proceed automatically with little CPU intervention required.

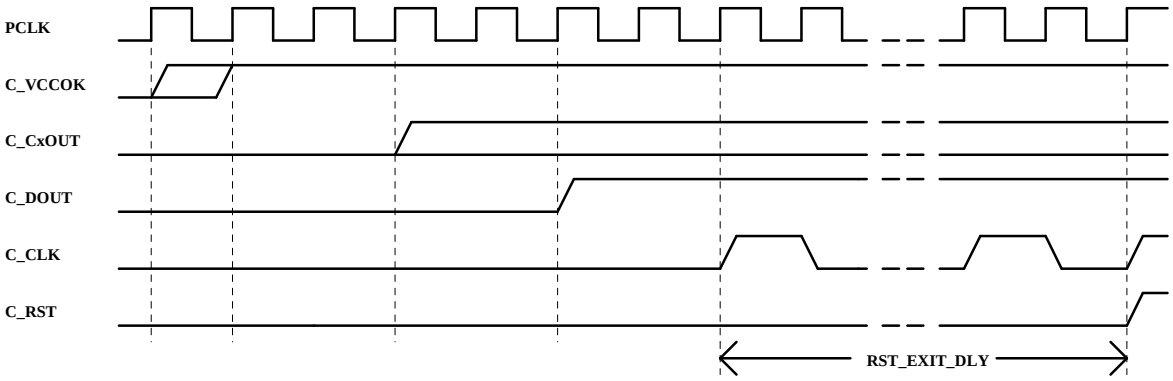
Listed in the table below are the default time values for the ISO7816 UART:

Constant Name	Function	Default Value
RST_EXIT_DLY	Cold Reset C_RST Low Width	40,000 C_CLK cycles
WARM_EXIT_DLY	Warm Reset C_RST Low Width	40,000 C_CLK cycles
IO_OPEN_DLY	ATR Early Response Limit	380 C_CLK cycles
IO_CLOSE_DLY	ATR Maximum Response Limit	40,000 C_CLK cycles
TS_FAIL_DLY	Maximum TS Start Delay	42,001 C_CLK cycles
CLK_STRT_DLY	C_DIN High to C_CLK Stop Delay	1860 C_CLK cycles min.
CLK_STOP_DLY	C_CLK Start to C_DIN Low Delay	700 C_CLK cycles
CLK_OFF_DLY	C_RST Low to C_CLK Off Delay	16 C_CLK cycles
IO_OFF_DLY	C_CLK Off Delay to C_DOUT Low Delay	16 C_CLK cycles
VCC_OFF_DLY	C_DOUT Low to C_VCCON Low Delay	16 C_CLK cycles
T0_GUARD_DLY	T=0 Protocol Guard Time	16 etu min.
T1_BGT	T=1 Protocol Block Guard Time	16 etu min.

The time values related to card deactivation, CLK_OFF_DLY, IO_OFF_DLY, and VCC_OFF_DLY are not specified in either the ISO/IEC or EVM standards, so these values are somewhat arbitrary, and can be modified without violating anything in these standards.

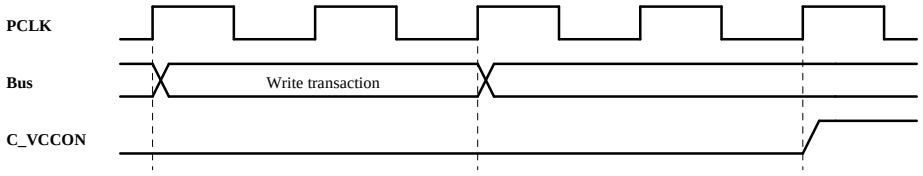
In all of the figures in this section the C_CLK divisor is assumed to be 0x00, just to make the diagrams easier to follow. Delays or signals referenced to PCLK are independent of the C_CLK divisor value.

The figure below shows the timing for card start-up in response to the V_VCCOK signal becoming active. The rising edge of the C_VCCOK signal is synchronized with PCLK and then initializes the internal C_CLK divider, so that this startup timing is independent of the C_CLK divisor value.

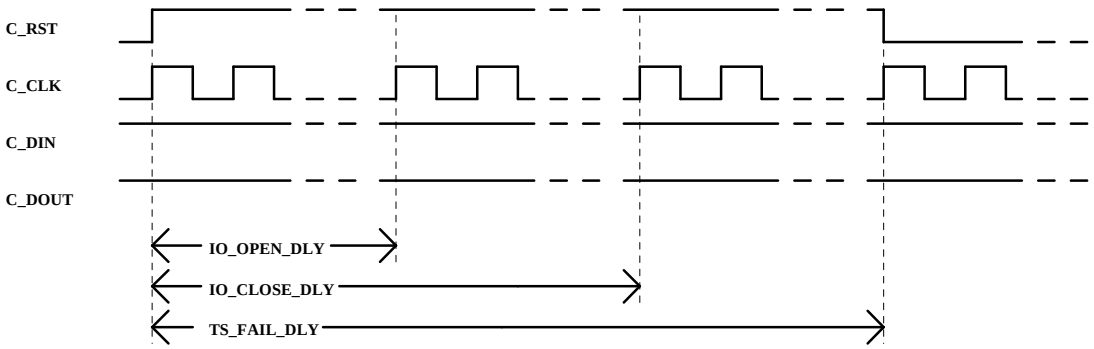


The figure below shows the timing of the C_VCCON signal relative to the bus write that starts the card activation sequence. This write initializes the internal C_CLK divider, for consistent timing.

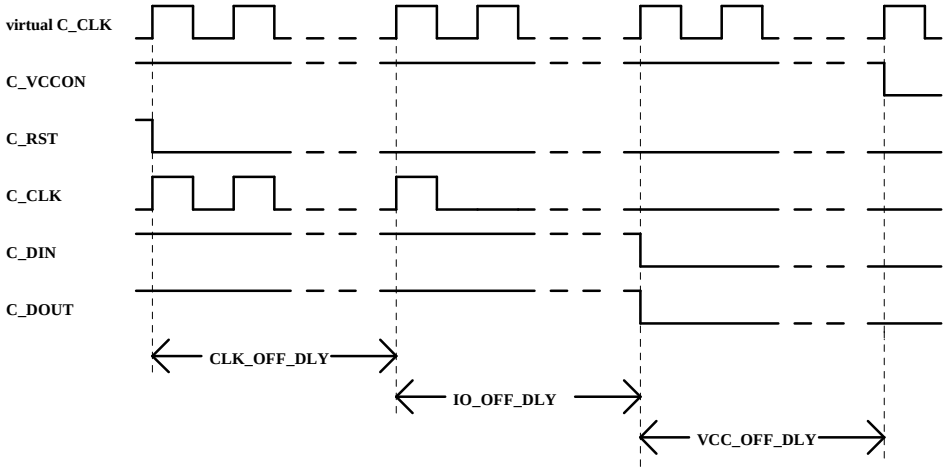
There is no constraint on the amount of time between the C_VCCON signal going active and the C_VCCOK signal becoming active, because this time is a function of the power supply for the card. Software is responsible for setting a time limit while waiting for the card activation to complete.



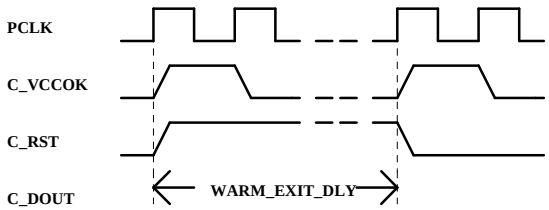
The figure below shows the timing for the Answer-To-Reset (ATR) sequence, which occurs at the end of either a Cold Reset or a Warm Reset. If the character TS starts during the IO_OPEN_DLY time, it will be reported as an early answer, and the receiver will not recognize the start of this character until this delay has expired. A normal response, consisting of both character TS and character T0, should be received before the IO_CLOSE_DLY time has passed. If the character TS has not started before the TS_FAIL_DLY time has passed, the deactivation sequence will be automatically started.



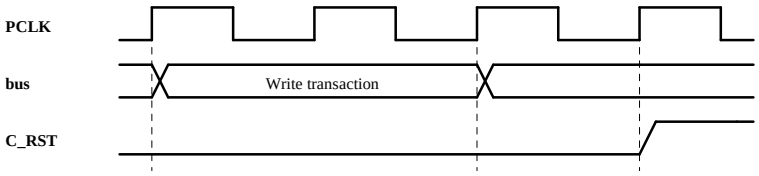
The figure below shows the timing for the deactivation sequence. As mentioned previously, these three delay times are not specified in either the ISO/IEC or EVM specification.



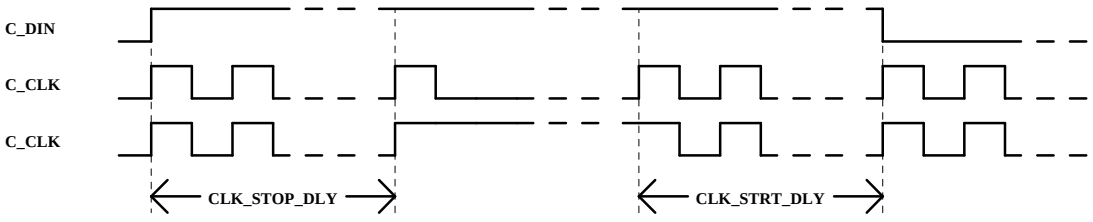
The figure below shows the timing for the Warm Reset sequence. The protocol state machine will not start a Warm Reset sequence until the reception of the character T0 (error-free) is complete.



The figure below shows the timing of the C_RST signal relative to the write that starts the Warm Reset sequence. This figure shows the earliest possible activation of the C_RST signal. The exact delay depends on the C_CLK divisor, because the C_RST signal is synchronized to a rising edge on the C_CLK signal.



The figure below shows the timing for stopping the clock. In addition to the timing requirement relative to the C_DIN signal, the protocol state machine does not allow the clock to stop at any time while a character is being received or transmitted. This allows the Clock Control Register to be written during the final character transfer before the clock is to be stopped. The C_CLK signal can be stopped in either state, under program control.



This page intentionally left blank.

Programming Interface

Registers

Register Name	Mnemonic	I/O address	R/W	Reset
Master Control Register	MCR	0x00	R/W	00000000
Direct Control/Status Register	DCSR	0x01	R/W	00000000
Clock Divisor Register	CDR	0x02	R/W	00000000
Clock Control Register	CCR	0x03	R/W	00000000
ETU Width Register	EWR	0x04	R/W	00000000
ETU Divider Register	EDR	0x05	R/W	00001100
FIFO Control Register	FCR	0x06	R/W	00000000
Parity Error Limit Register	PELR	0x07	R/W	01110111
Time Constant 0, Byte 0 Register	TC00R	0x08	R/W	01011111
Time Constant 0, Byte 1 Register	TC01R	0x09	R/W	00100111
Time Constant 0, Byte 2 Register	TC02R	0x0A	R/W	00000000
Guard Time Register	GTR	0x0B	R/W	11111111
Time Constant 1, Byte 0 Register	TC10R	0x0C	R/W	11111111
Time Constant 1, Byte 1 Register	TC11R	0x0D	R/W	01001010
Time Constant 1, Byte 2 Register	TC12R	0x0E	R/W	00000000
Timer Control Register	TCR	0x0F	R/W	00000000
Master Mode Register	MMR	0x10	R/W	00000000
Power Control Register	PCR	0x11	R/W	00000000
Protocol State Register	PSR	0x12	R	00000001
UART Status Register	USR	0x13	R	00000000
Protocol Interrupt Enable Register	PIER	0x14	R/W	00000000
UART Interrupt Enable Register	UIER	0x15	R/W	00000000
Parity Error Status Register	PESR	0x17	R	00000000
Alternate Protocol State	APSR	0x1A	R	00000001
Alternate UART Status	AUSR	0x1B	R	00000000
UART Buffer Register	UBR	0x1C	R&W	xxxxxxxx
Version Register	VR	0x1E	R	00000000
Master Reset Register	MRR	0x1F	R/W	00000001

Register Descriptions

Master Control Register (MCR) (Address = 0x00)			
Bit(s)	**Value**	**Description**	
7	0	Normal UART operation.	
	1	Bypass operation. In this mode all card interface signals are under direct program control. For security reasons, bypass operation only works while the protocol state machine is in the inactive state.	
6		This bit is reserved and should always be written with zero.	
5	0	Normal operation	
	1	Deactivate if initial character TS is not 0x3B (direct convention) or 0x3F (inverse convention) or either (automatic convention detection enabled). Deactivate if parity error limit is reached before valid character TS is received.	
4	0	Normal operation	
	1	Deativate in case of parity error (receive or transmit). Primarily for use during Answer-To-Reset (ATR). Should only be used in protocol T=0.	
3	0	Disable automatic automatic convention detection. In this case the convention must be set by software before starting the activation sequence.	
	1	Enable automatic convention detection during the initial character TS. In this mode the protocol state machine will automatically select the convention and the character TS will not be transferred to the receive buffer. No receive buffer interrupt will be generated for the character TS.	
2	0	Direct convention: Serial data is LSB first and normal polarity. With automatic convention detection, this bit is set by the hardware based on the contents of the initial character TS.	
	1	Inverse convention: Serial data is MSB first and inverted polarity.	
1	0	Read	Warm Start completed.
		Write	No effect.
	1	Read	Warm Start in progress.
		Write	Setting this bit initiates a Warm Start. This bit is ignored if the protocol state machine is not in the "active" state. The protocol state machine automatically does a warm start if there is no Answer-to-Reset.
0	0	Read	Deactivation process in progress or completed.
		Write	Clearing this bit starts the card deactivation process. The deactivation process can be started at any time. If either C_VCCOK or C_PRES go inactive the deactivation process will be initiated.
	1	Read	Activation process in progress or completed.
		Write	Setting this bit initiates the card activation process.

Direct Control/Status Register (DCSR) (Address = 0x01)			
Bit(s)	**Value**	**Description**	
7:1	Write	The state of the various card signals will only be affected if both th C_VCCON and C_VCCOK signals are active. This guarantees that all card signals will be Low during card insertion.	
7	Read	Reports the current state of the C_C8IN (C8) pin on the card interface.	
	Write	Sets the state of the C_C8OUT (C8) pin on the card interface.	
6	Read	Reports the current state of the C_DIN (C7) pin on the card interface.	
	Write	Normal	No effect.
		Bypass	Sets the state of the C_DOUT (C7) pin on the card interface.
5	Read	Reports the current state of the C_C6IN (C6) pin on the card interface.	
	Write	Sets the state of the C_C6OUT (C6) pin on the card interface.	
4	Read	Reports the current state of the C_PRES signal.	
	Write	No effect.	
3	Read	Reports the current state of the C_C4IN (C4) pin on the card interface.	
	Write	Sets the state of the C_C4OUT (C4) pin on the card interface.	
2	Read	Reports the current state of the C_CLK (C3) pin on the card interface.	
	Write	Normal	No effect.
		Bypass	Sets the state of the C_CLK (C3) pin on the card interface.
1	Read	Reports the current state of the C_RST (C2) pin on the card interface.	
	Write	Normal	No effect.
		Bypass	Sets the state of the C_RST (C2) pin on the card interface.
0	Read	Reports the current state of the C_VCCOK signal..	
	Write	Normal	No effect.
		Bypass	Sets the state of the C_VCCON pin on the card interface.

Clock Divisor Register (CDR) (Address = 0x02)		
Bit(s)	**Value**	**Description**
7:0		Time constant for the C_CLK divider. The C_CLK frequency is the PCLK frequency divided by 2*n. In other words, the C_CLK signal is High for “n” PCLK cycles and Low for “n” PCLK cycles. The time constant should only be changed while the card is inactive or while both the UART and the card are in the receive state. A time constant of 0x00 operates the same as 0x01. The C_CLK divider will never generate "runt" output pulses.

Clock Control Register (CCR) (Address = 0x03)		
Bit(s)	**Value**	**Description**
7:2		These bits are ignored when written, and always return zeros when read.
1	0	The C_CLK signal runs continuously, or start the C_CLK signal. Hardware automatically enforces the C_CLK start-to-next character delay when starting up the C_CLK signal.
	1	Stop the C_CLK signal after character transmission or reception. Hardware automatically enforces the character-to-C_CLK stop delay. This bit may be set at any time during or after the last character transfer.
0	0	When stopping the C_CLK signal, stop with the C_CLK signal in the Low state.
	1	When stopping the C_CLK signal, stop with the C_CLK signal in the High state.

ETU Width Register (EWR) (Address = 0x04)		
Bit(s)	**Value**	**Description**
7:1		These bits are ignored when written, and always return zeros when read.
0	0	ETU is 31 cycles of the ETU divider output. This is the default value.
	1	ETU is 32 cycles of the ETU divider output.

ETU Divider Register (EDR) (Address = 0x05)		
Bit(s)	**Value**	**Description**
7:0		Time constant for the ETU generator. This generator counts the C_CLK signal modulo n. A time constant of 0x00 operates the same as 0x01. The default value is 0x0C, for an ETU that is 372 (31 x 12) clocks.

FIFO Control Register (FCR) (Address = 0x06)		
Bit(s)	**Value**	**Description**
7	0	No effect.
	1	Purge FIFO. Also clears the Parity Error and Overrun status bits.
6:4	000	Signal FIFO full with one byte in buffer. This selection is forced internally in the T=0 protocol mode because of the way that parity errors are handled.
	001	Signal FIFO full with two bytes in buffer.
	010	Signal FIFO full with three bytes in buffer.
	011	Signal FIFO full with four bytes in buffer.
	100	Signal FIFO full with five bytes in buffer.
	101	Signal FIFO full with six bytes in buffer.
	110	Signal FIFO full with seven bytes in buffer.
	111	Signal FIFO full with eight bytes in buffer.
3:0	Read	Reports the number of bytes available in the receive buffer. Valid values are 0000 (buffer is empty) to 1000 (buffer contains eight bytes). No value outside this range will ever be returned.
	Write	No effect.

Parity Error Limit Register (PELR) (Address = 0x07)		
Bit(s)	**Value**	**Description**
7	0	No effect.
	1	Clear the retry counter. Should only be used in the NAK Error interrupt service routine to avoid interfering with the error counting.
6:4		Number of retries allowed on a character transmission that is NAKed by the card. 000 selects no retries, 111 selects seven retries. A retransmit starts after 15 ETU. If the number of retries is matched without a successful ACK, a parity error interrupt will be generated. Used only in protocol T=0.
3	0	No effect.
	1	Clear the parity error counter counter. Should only be used in the Parity Error interrupt service routine to avoid interfering with the error counting.
2:0		Allowed number of received parity errors on a character before requesting a parity error interrupt. 000 selects interrupt on first parity error, 111 selects interrupt on eighth parity error. Used only in protocol T=0.

Time Constant 0, Byte 0 Register (TC00R) (Address = 0x08) Time Constant 0, Byte 1 Register (TC01R) (Address = 0x09) Time Constant 0, Byte 2 Register (TC02R) (Address = 0x0A)		
Bit(s)	**Value**	**Description**
7:0		Byte of time constant for Timer 0. Timer 0 counts ETUs.

Guard Time Register (GTR) (Address = 0x0B)			
Bit(s)	**Value**	**Description**	
7:0		Guard Time (in number of ETUs) from the start of one transmit character to the start of the next transmit character. This value is an unsigned number.	
		T=0	Guard Time is value + 13. Special case of 0xFF selects 12 ETU.
		T=1	Guard Time is value + 12. Special case of 0xFF selects 11 ETU.

Time Constant 1, Byte 0 Register (TC10R) (Address = 0x0C) Time Constant 1, Byte 1 Register (TC11R) (Address = 0x0D) Time Constant 1, Byte 2 Register (TC12R) (Address = 0x0E)		
Bit(s)	**Value**	**Description**
7:0		Byte of time constant for Timer 1. Timer 1 counts ETUs.

Timer Control Register (TCR) (Address = 0x0F)		
Bit(s)	**Value**	**Description**
7		This bit is reserved and should always be written with zero.
6:5	00	Timer 1 continuous count. Reload on terminal count.
	01	Timer 1 start on next start bit, continuous count until disabled. Reload on terminal count.
	10	Timer 1 start on next start bit, continuous count until subsequent start bit, then stop.
	11	Timer 1 start on next start bit, reload on all subsequent start bits or terminal count.
4	0	Disable Timer 1.
	1	Enable Timer 1. Changing this bit from zero to one loads the time constant in preparation for counting down.
3		This bit is reserved and should always be written with zero..
2:1	00	Timer 0 continuous count. Reload on terminal count.
	01	Timer 0 start on next start bit, continuous count until disabled. Reload on terminal count.
	10	Timer 0 start on next start bit, continuous count until subsequent start bit, then stop.
	11	Timer 0 start on next start bit, reload on all subsequent start bits or terminal count.
0	0	Disable Timer 0.
	1	Enable Timer 0. Changing this bit from zero to one loads the time constant in preparation for counting down.

Master Mode Register (MMR) (Address = 0x10)		
Bit(s)	**Value**	**Description**
7:3		These bits are ignored when written, and always return zeros when read.
2	0	Receive Mode.
	1	Transmit Mode. Setting this bit to one automatically switches MSR[0] to report Transmit Buffer Empty status in MSR[0] and will generate in interrupt if enabled in the UIER. This bit can only be set while the UART is in the Active state.
1	0	Software-controlled Transmit/Receive operation.
	1	Automatically enter Receive Mode (and clear MMR[2]) after the next transmit character that is not NAKed. This bit is also automatically cleared after the next transmit character. This bit can only be set while the UART is in the Active state.
0	0	Protocol T=0. Character transfer includes an error-signal response. There is no receive FIFO in this mode.
	1	Protocol T=1. Character transfers do not include an error-signal response. This option should be selected during the ATR character transfers to inhibit any error-signal response.

Power Control Register (PCR) (Address = 0x11)		
Bit(s)	**Value**	**Description**
7:2		This bits are ignored when written, and always returns zeros when read.
1:0	00	C_VCC50 output is High, to select 5.0V for card power supply.
	01	This bit combination is reserved and should not be used.
	10	C_VCC30 output is High, to select 3.0V for card power supply.
	11	C_VCC18 output is High, to select 1.8V for card power supply.

Protocol State Register (PSR) (Address = 0x12) Alternate Protocol State Register (APSR) (Address = 0x1A)			
Bit(s)	**Value**	**Description**	
7:0	Read	PSR	Read operation clears Protocol Interrupt-Pending status.
		APSR	Read operation does not clear Protocol Interrupt-Pending Status.
	0x80	Active state. Card is active, with characters TS and T0 complete.	
	0x40	Waiting-For-T0 state. Card is active, and either waiting for or receiving the character T0.	
	0x20	Waiting-For-TS state. Card is active, and either waiting for or receiving the character TS.	
	0x10	Activation/Reset state. Card power on and powered. RST is Low.	
	0x08	Waiting-For-Power state. Card power on, waiting for VCCOK.	
	0x04	Deactivation state. Card is being deactivated.	
	0x02	Activation-Timeout state. Card did not respond with ATR within window, waiting to start deactivation.	
	0x01	Power-Off state. Card power is off, and all card signals are Low.	

UART Status Register (USR) (Address = 0x13) **Alternate UART Status Register (AUSR) (Address = 0x1B)**			
Bit(s)	**Value**	**Description**	
7:1	Read	USR	Read operation clears these status bits.
		AUSR	Read operation does not affect these status bits.
7	0	No Timer 1 terminal count.	
	1	Timer 1 reached its terminal count.	
6	0	No Timer 0 terminal count.	
	1	Timer 0 reached its terminal count.	
5	0	No Early Answer to reset.	
	1	Early Answer to reset (less than 368 C_CLK cycles after C_RST rising edge.)	
4	0	No Parity Error.	
	1	T=0	Character received with parity error a number of times matching the programmed limit. Characters with parity errors are not loaded into the buffer. This bit is cleared by a FIFO purge.
		T=1	All receive characters are loaded to the buffer. This bit reports the result of the parity check for each character. This bit is automatically cleared by a FIFO purge.
3	0	No NAK Error.	
	1	T=0	Character was NAKed the number of times matching the programmed limit.
		T=1	This bit is not used.
2	0	No Overrun detected.	
	1	The receive buffer has been overrun, and at least one character has been lost. This bit is automatically cleared by a FIFO purge. The receive buffer is always eight bytes deep, so an overrun cannout occur until the ninth character is received without a buffer read. Only the affected byte is marked as having been overrun.	
1	0	No change in the state on the C_PRES signal.	
	1	The C_PRES signal changed state.	
0	0	Rx	Receive buffer is not full to programmed depth.
		Tx	Transmit buffer is full. In protocol T=0 this bit will remain set until the byte is either sucesssfully transmitted or until the programmed number of NAKs is reached.
	1	Rx	Receive buffer is full to programmed depth.
		Tx	Transmit buffer is empty.

Protocol Interrupt Enable Register (UIER) (Address = 0x14)		
Bit(s)	**Value**	**Description**
7	0	Disable interrupt on entering Active state.
	1	Enable interrupt on entering Active state.
6	0	Disable interrupt on entering Waiting-For-T0 state.
	1	Enable interrupt on entering Waiting-For-T0 state.
5	0	Disable interrupt on entering Waiting-For-TS state.
	1	Enable interrupt on entering Waiting-For-TS state.
4	0	Disable interrupt on entering Activation/Reset state.
	1	Enable interrupt on entering Activation/Reset state.
3	0	Disable interrupt on entering Waiting-For-Power state.
	1	Enable interrupt on entering Waiting-For-Power state.
2	0	Disable interrupt on entering Deactivation state.
	1	Enable interrupt on entering Deactivation state.
1	0	Disable interrupt on entering Activation-Timeout state.
	1	Enable interrupt on entering Activation-Timeout state.
0	0	Disable interrupt on entering Power-Off state.
	1	Enable interrupt on entering Power-Off state.

UART Interrupt Enable Register (PIER) (Address = 0x15)		
Bit(s)	**Value**	**Description**
7	0	Disable interrupt on Timer 1 terminal count.
	1	Enable interrupt on Timer 1 terminal count.
6	0	Disable interrupt on Timer 0 terminal count.
	1	Enable interrupt on Timer 0 terminal count.
5	0	Disable interrupt on Early Answer To Reset
	1	Enable interrupt on Early Answer To Reset
4	0	Disable interrupt on Parity Error.
	1	Enable interrupt on Parity Error.
3	0	Disable interrupt on NAK Error.
	1	Enable interrupt on NAK Error.
2	0	Disable interrupt on Overrun Error.
	1	Enable interrupt on Overrun Error.
1	0	Disable interrupt on C_PRES signal transition.
	1	Enable interrupt on C_PRES signal transition.
0	0	Disable interrupt on Receive Buffer Full or Transmit Buffer Empty.
	1	Enable interrupt on Receive Buffer Full or Transmit Buffer Empty.

Parity Error Status Register (PESR) (Address = 0x17)		
Bit(s)	**Value**	**Description**
7		This bit is ignored when written, and always returns zero when read.
6:4	Read	Current number of NAKs received on character being transmitted. Used only in protocol T=0.
3		This bit is ignored when written, and always returns zero when read.
2:0	Read	Current number of received parity errors on character being received. Used only in protocol T=0.

UART Buffer Register (UBR) (Address = 0x1C)		
Bit(s)	**Value**	**Description**
7:0	Read	Returns the contents of the Receive Buffer, and removes this character from the buffer.
	Write	Loads the Transmit Buffer with a character for transmission. Transmission will start as soon as allowed by the various time limits (CWT and BWT).

Version Register (VR) (Address = 0x1E)		
Bit(s)	**Value**	**Description**
7:0	Read	Returns an 8-bit version identifier. Currently 0x00, set at compile time.

Master Reset Register (MRR) (Address = 0x1F)		
Bit(s)	**Value**	**Description**
7:1		These bits are ignored during writes and will always return zeros when read.
0	0	Normal operation.
	1	Reset all control registers while this bit is set. Bit must be cleared before attempting to write to other registers.

Protocol Constants

Protocol timer values are set by logic-synthesis-time values that are consistent with the EVM specification. If your application does not require EVM compliance, these values can be changed before logic synthesis time. These constants can also be replaced by programmable values if required.

Shown below are the constants from the Verilog file used in the design:

```
  `define RST_EXIT_DLY  16'h9c40                    /* 40000  RST Low Width         */
  `define RST_EXIT_TST  16'h0040                    /*    64  RST Low Width         */

  `define WARM_EXIT_DLY 16'h9c40                    /* 40000  Warm RST Low Width    */
  `define WARM_EXIT_TST 16'h0040                    /*    64  Warm RST Low Width    */

  `define IO_OPEN_DLY    9'h17b                     /*   380  I/O Min Delay         */
  `define IO_CLOSE_DLY  16'h9c3f                    /* 40000  I/O Max Delay         */
  `define TS_FAIL_DLY   16'ha410                    /* 42001  Max TS Start Delay    */

  `define CLK_STOP_DLY  11'h743                     /*  1860  I/O High to CLK stop  */
  `define CLK_STRT_DLY  11'h2bb                     /*   700  CLK Start to I/O Low  */

  `define CLK_OFF_DLY    5'h0f                      /*    16  RST Off to CLK Off    */
  `define IO_OFF_DLY     5'h0f                      /*    16  CLK Off to I/O Low    */
  `define VCC_OFF_DLY    5'h0f                      /*    16  I/O Low to VCC Off    */


  `define T0_GUARD_DLY   5'h10                      /*    16  strt-strt opp dir     */
  `define T1_BGT         5'h16                      /*    22  block guard time      */

/*********************************************************************************************/
/*  default bit rate                                                                         */
/*********************************************************************************************/
  `define DBIT             744                      /*   744  PCLK/bit              */
  `define DBITH            372                      /*   372  PCLK/half-bit         */
  `define BRATE             31                      /*   rate integer               */
  `define BDIV              12                      /*   divide integer             */
```

Verilog Top Level

Shown below are the top-level Verilog connections:

```
module iso7816 (C_C4OUT, C_C6OUT, C_C8OUT, C_CLK, C_DOUT, C_RST, C_VCC18, C_VCC30,
                C_VCC50, C_VCCON, ETU_PLS, PINT_REQ, PRDATA, C_C4IN, C_C6IN, C_C8IN,
                C_DIN, C_PRES, C_VCCOK, PADDR, PCLK, PENABLE, PRESETB, PSEL, PWDATA,
                PWRITE, TEST_EN);

  input         C_C4IN;                                 /* card C4 connector input      */
  input         C_C6IN;                                 /* card C6 connector input      */
  input         C_C8IN;                                 /* card C8 connector input      */
  input         C_DIN;                                  /* card data input              */
  input         C_PRES;                                 /* card present                 */
  input         C_VCCOK;                                /* card power okay              */
  input         PCLK;                                   /* peripheral bus clock         */
  input         PENABLE;                                /* peripheral enable            */
  input         PRESETB;                                /* master reset                 */
  input         PSEL;                                   /* peripheral select            */
  input         PWRITE;                                 /* peripheral write enable      */
  input         TEST_EN;                                /* test mode enable             */
  input   [4:0] PADDR;                                  /* peripheral address bus       */
  input   [7:0] PWDATA;                                 /* peripheral write data bus    */
  output        C_C4OUT;                                /* card C4 connector output     */
  output        C_C6OUT;                                /* card C6 connector output     */
  output        C_C8OUT;                                /* card C8 connector output     */
  output        C_CLK;                                  /* card clock                   */
  output        C_DOUT;                                 /* card data output             */
  output        C_RST;                                  /* card reset                   */
  output        C_VCC18;                                /* card voltage 1.8V select     */
  output        C_VCC30;                                /* card voltage 3.0V select     */
  output        C_VCC50;                                /* card voltage 5.0V select     */
  output        C_VCCON;                                /* card power enable            */
  output        ETU_PLS;                                /* etu timing clock             */
  output        PINT_REQ;                               /* interrupt request            */
  output  [7:0] PRDATA;                                 /* peripheral read data bus     */
```