

Clock Spectrum Spreader



Features

Optimal spectrum spreading algorithm

Requires a 0.5nS delay cell, but the absolute value is not critical

Process-tolerant design

Three options for spectrum spread

Works by adding 0, +0.5nS, -0.5nS, +1.0nS or -1.0nS during each clock cycle

Average clock cycle length is unchanged

Description

The clock spectrum spreader is inserted in the clock path. When enabled, it modifies the clock cycle time by 0, +/-0.5nS or +/-1.0nS on a cycle-by-cycle basis according to a specific profile. This profile creates the optimal spreading of the spectrum of the clock. Although individual clock cycles vary by one of these amounts, the average clock cycle time is unchanged.

For example, with a 50MHz base clock frequency (20nS clock period) the instantaneous frequency will vary between 52.6MHz (19nS) and 47.6MHz (21nS).

Interface

```
module dith_top (osc_hss, gcm0_reg, gcm1_reg, osc_hs, resclk8b);  
  
    input  [1:0] gcm0_reg;    /* dither mode select          */  
    input      gcm1_reg;    /* dither enable              */  
    input      osc_hs;      /* high-speed oscillator direct output */  
    input      resclk8b;    /* reset pulse (synchronous with negedge osc_hs) */  
    output     osc_hss;     /* dithered osc output        */  
endmodule
```