Y180

8-bit Microprocessor Synthesizable Verilog HDL Model

* Fully functional synthesizable Verilog HDL model of the Z80180™ CPU
* Vendor and technology independent
* Software compatible with several industry-standard processors
* 181 Instructions, plus an undefined opcode trap
* Eight addressing modes
* 64K byte addressing capability
* 8 bit ALU with bit, byte and BCD operations
* 8x8 multiply instruction
* Powerful vectored interrupt capability
* Static, fully synchronous design
* Designed without 3-state busses
* Easily modified external interface
* Architectural upgrade path to 16 or 32 bits possible

A	F
B	C
D	E
H	L
IX	
IY	

A'	F'
B'	C'
D'	E'
H'	L'

I	R

SP
PC

CPU registers

Use the Y180 model, along with any necessary application-specific logic, to create your own proprietary product. Or customize the CPU hardware or instruction set to handle unique application requirements. Then, with the technology-independent nature of the Y180 model, take your design to the ASIC vendor of your choice.